

Notice of References Cited

Application/Control No.

09/768,911

Applicant(s)/Patent Under
Reexamination
CHOW ET AL.

Examiner

David A. Zarneke

Art Unit

2827

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
*	N	JP 61-147551	07-1986	Japan	Kano	
*	O	WO 98/57373	12-1998	WO	Kowalski	
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, Silicon Processing for the VLSI Era-Volume 2:Process Integration, Lattice Press, 1990, pp. 194-199, 387, 482 and 508
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.